



PHILIPS

1246

SERVICE

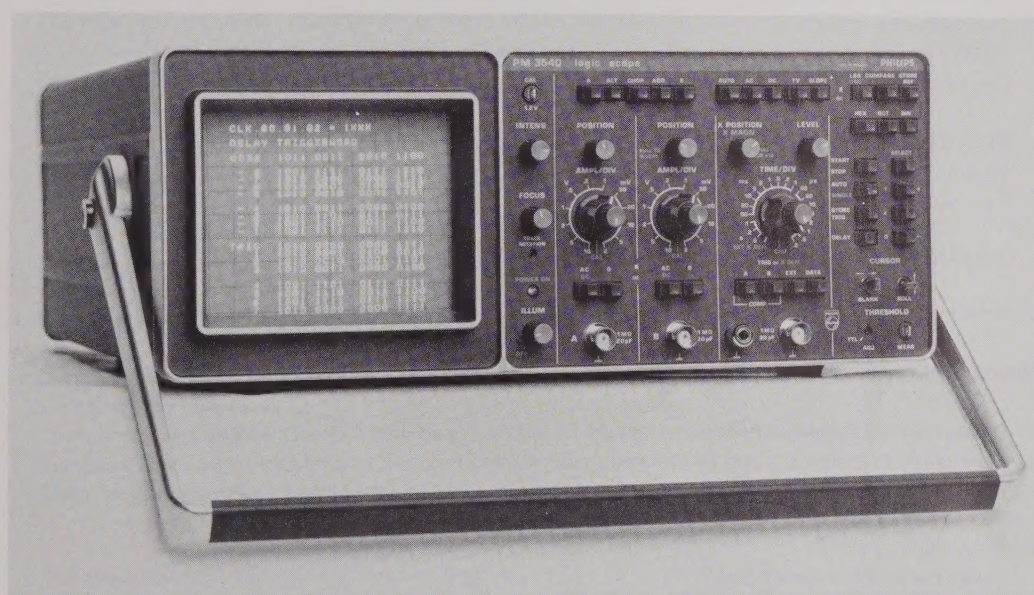
Scientific & Analytical Equipment
Test & Measuring Instruments
Industrial Controls
Welding
Industrial Data-processing Systems

Scientific &
Industrial
Equipment
Division

80.08.01

TEST AND MEASURING EQUIPMENT

DTE 1



16 Channel logic scope
16 Kanal logik-Oszilloskop
Oscilloscope logique 16 voies
PM3540

Subject: Software alteration in versions/03 and onwards.
Already published: none.

9499 508 01111

CONTENTS

1. GENERAL INFORMATION
 - 1.1. Introduction
 - 1.2. Negative logic
 - 1.3. Service selftest routine
 - 1.4. Summary of tests
2. DESCRIPTION OF THE SERVICE TESTS
 - 2.1. Power-up test
 - 2.2. Functional test mode
 - 2.3. Failure tracing via the selftest
 - 2.4. Hints for detection faults in circuitry not covered by the selftest
3. SIGNATURE ANALYSIS MODE
 - 3.1. General information
 - 3.2. Selection of the S.A. mode
 - 3.3. Connections and settings
 - 3.4. Failure tracing with S.A.
 - 3.5. List of signatures
4. TESTING MICRO-PROCESSOR AND ADDRESS BUS
 - 4.1. Free-running
 - 4.2. Free-running test set-up
5. MANUAL CONSEQUENCES DUE TO MODIFICATIONS

LIST OF FIGURES

- Fig. 1. Flow chart of the test procedure
- Fig. 2. Flow chart of the tests 2 and 3
- Fig. 3. Flow chart of test 4
- Fig. 4. Flow chart of test 5
- Fig. 5. Flow chart of test 6
- Fig. 6. Flow charts of the tests 7 and 8
- Fig. 7. Free-running
- Fig. 8. Free-running test set-up (Mechanical)
- Fig. 9. Free-running test set-up (Electrical)
- Fig. 10. Micro-processor p.c. board

1. GENERAL INFORMATION

1.1. INTRODUCTION

From version /03 the logic scope PM 3540 is provided with the facility of measuring negative logic signals, to this end the soft-ware has to be altered. Furthermore the service selftest is modified to enable signature analysis measurement.

At the same time the band-width of the oscilloscope part of the PM 3540 is increased from 25 MHz to 35 MHz. The consequences of these alterations in the manual are dealt with in section 5 of this supplement.

1.2. NEGATIVE LOGIC

The negative logic mode is selected by pressing the 0/— pushbutton and is indicated by the message INV, given in the heading of the display. In this mode, the contents of the data input memory is complemented (see also flow chart fig. 3.9. in the manual).

For returning to the "normal" mode, the 1/+ pushbutton has to be pressed.

1.3. SERVICE SELFTEST ROUTINE

The service selftest routine consists of 7 test modules (test 2 ... test 8) to facilitate isolating functional faults in various parts of the analyzer circuitry. The service selftest can be used in two different modes:

1.3.1. Functional test mode by which each selected test module tests the functions of a marked out circuit section.

1.3.2. Signature analysis mode to facilitate tracing faults on component level by analyzing signatures generated by the selftest routine itself.

To do this a Signature Analyzer has to be connected to the faulty circuit to compare signatures taken with the Signature Analyzer to those signatures contained in this supplement.

There is one repeatable signature per node.

The recommended procedure of tracing faults is:

- locate the circuitry section where the fault occurs by observing the messages in the display when a test module is called.

To optimize your diagnosis, it is recommended that the seven tests are completed.

- trace the failure in the located circuitry section by means of signature analysis in the procedure as described before.

1.4. SUMMARY OF TESTS (OR MODULES)

Test 1: Power-up test (not visible, not manipulateable)

Test 2: Delay counter

Test 3: Delay counter, loaded with inverted values as test 2.

Test 4: Address-counter of data input RAM's

Test 5: Data input RAM's

Test 6: Data input circuitry

Test 7: Trigger RAM's

Test 8: Trigger RAM's, loaded with inverted values as test 7.

2. DESCRIPTION OF THE SERVICE TESTS

2.1. POWER-UP TEST (Test 1)

Every time the instrument is switched-on, the micro-processor executes the power-up test, which consists of:

- PROM test (i.e. a check-sum test)
- Scratch-pad RAM test (i.e. a write-read test).

Normally the display on the c.r.t. appears approximately 10 s after switching-on.

If no display, or only one dot appears, one of the possibilities is that the micro-processor remains in the PROM test. The micro-processor is then continuously checking the sum of stored information in the EPROM's. If the display shows an address, the instrument is looping in the RAM test. The micro-processor is continuously checking the address which delivers the faulty data (see Fig. 1).

2.2. FUNCTIONAL TEST MODE (Test 2 ... Test 8)

The selftest routine is selected by pressing STORE TRIG and STORE REF pushbuttons simultaneously, the logic scope enters the selftest program at test 2 (i.e. the first test module).

By pressing the START pushbutton the logic scope enters test 3 and so on until test 8. When START is pressed during test 8 the logic scope jumps to test 2 again (see Fig. 1).

Settings

- No external clock
- No input POD's connected
- No external trigger qualifier

Leaving the service routine is achieved by pressing the X pushbutton.

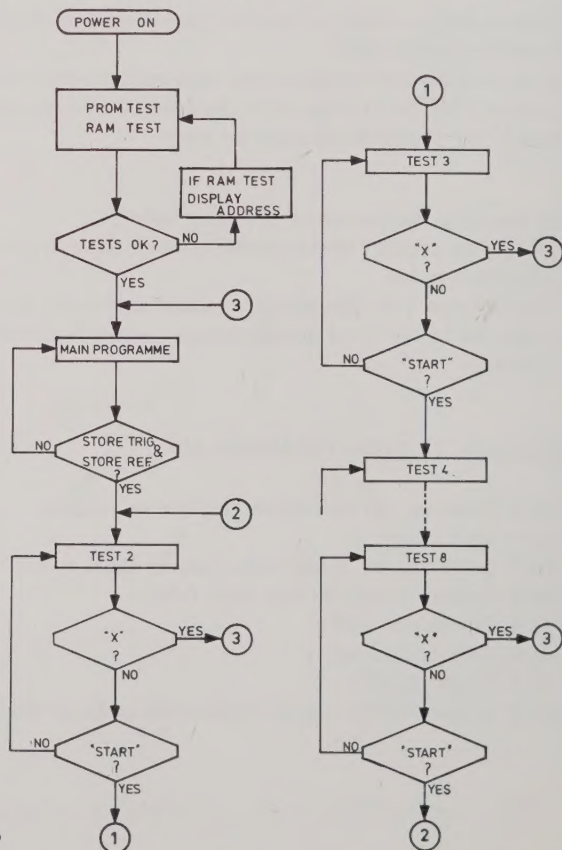


Fig. 1. Flow chart of the test procedure

2.2.1. Test 2 and 3. The delay counter D2024, D2026, D2027, D2028. See fig. 2.

The testmodule 2 enables a testing of the delay counter and the well functioning of the clockpulse generating hardware.

Test 2 has a counter preset of 6969.

Clockpulses are generated by the testmodule to count down the content of the delay counter. When the counter content becomes zero the "WRAM" signal will be reset resulting in a disabling of the clockpulses. On the display will be shown the text: "TEST 2 IS OK, CNT = ...".

The count is displayed in decimal digits and must be equal to the number given above for the preset.

If the "WRAM" fails to be reset then the counter will overflow. This is mentioned by the text: "TEST 2 FAILS" on the display.

If "SELECT" is depressed the module will be continuously repeated. Whether faulty or not. Eventually the overflow value 9984 will then be displayed.

In case the displayed count is not equal to the preset number, the counted result may be checked on the hardware by means of a logic scope.

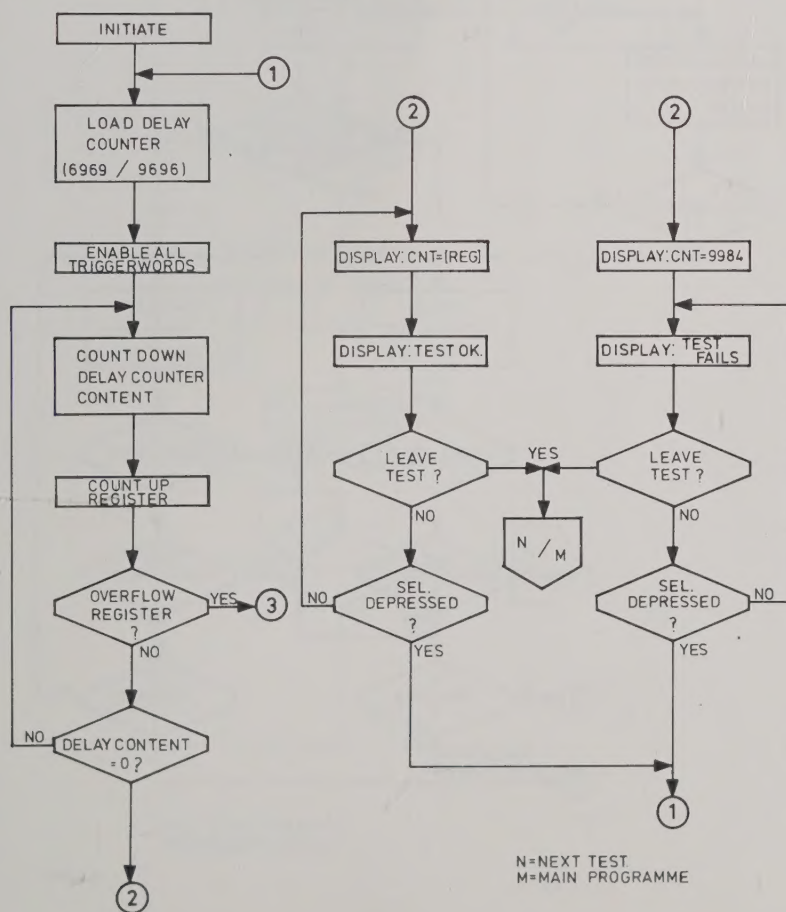
If the count appears to be higher than the measured one, either the clockpulse circuit failed or the counter did not accept all clockpulses. If it is lower, than a decade may produce false carries.

The clockpulse can be shown on an oscilloscope while "SELECT" is pressed. Probe at D2036, pin 5, for triggering the scope, probe at D2023, pin 5 (neg.) or pin 6 (pos.).

If no "SYSCL" pulses are present, check whether D2036, pin 12 is high. If not so, test the triggerword rams. Be sure that the "WRAM" control circuit operates correctly in case of overflow (test 6).

Note: The clock and qualifiers inputs must remain unconnected.

Test 3 is equivalent to test 2, but the counter preset is 9696.



TEST 2/3

MA10367

Fig. 2. Flow chart of the tests 2 and 3

2.2.2. Test 4. The dataram addresscounter. See fig. 3.

The addresscounter D2014 and D2017 can be tested by testmodule 4. The counter is loaded with a given value and the output address is compared with the input value.

The input value is incremented each time the loop is repeated.

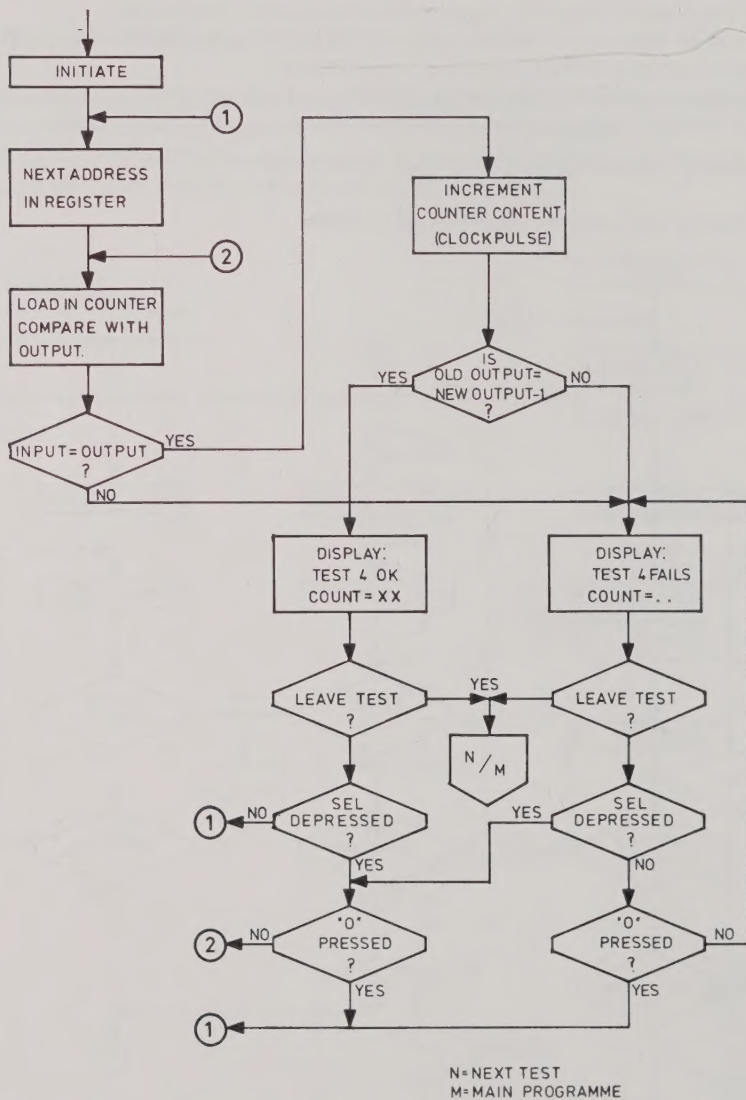
In order to pass through all possible input values when there is a discrepancy between input and output, a "TEST 4 FAILS" message will be displayed. The program stops at the last value being displayed in two hexadecimal digits.

As long as there is no failure observed, a "TEST 4 IS OK" message is displayed with unstable digits.

During the same run the counter is tested for clockpulse input. Two output values from before and after a clock-pulse are compared.

In case "SELECT" is depressed, the loop is always repeated with the last value unchanging. Pressing "0" makes the value move on by one step.

If failures occur, check first the clockpulse "SYSCL" to be caused by "CLDIM".



TEST 4

MA10368

Fig. 3. Flow chart of test 4

2.2.3. Test 5. Datarams. See fig. 4.

The datarams D2018 and D2019 are tested by means of testmodule 5. To this end the input terminals may be connected to any configuration of low and high levels, providing a wellknown and modifiable 16 bit data input signal. This input signal is then constantly loaded on all 64 addresses of the dataram.

The output of the dataram is read and displayed in four columns of 16 lines after the test "TEST 5" at the first line.

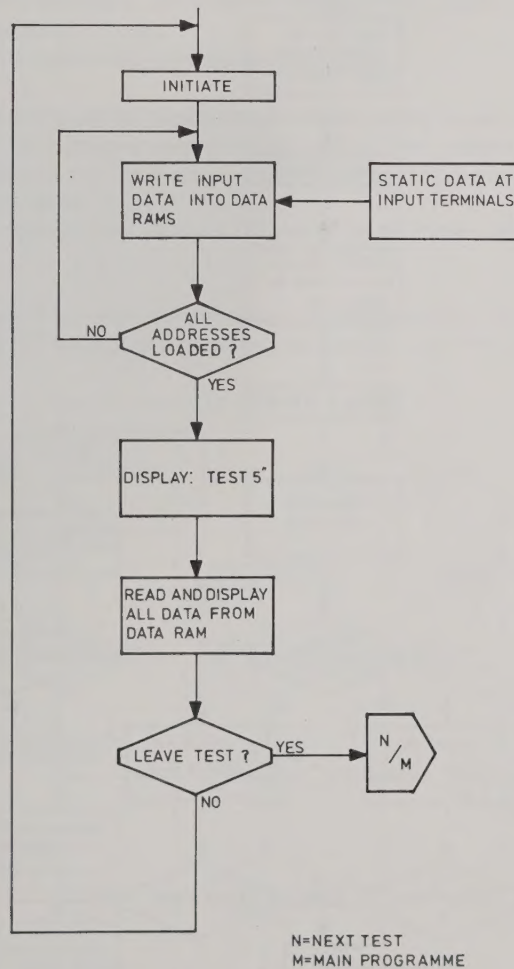
Each column contains 4 hex. digits of the 16 bit data word, the first column of the addresses 0-15. The second column of the addresses 16-31, etc.

Apart from "START/STOP" no switches are used in this module.

The test can only be implemented if the "WRAM" and the "SYSCL" signals are well functioning. The same holds for the address counter.

In case of failures, the output signals of the gates D2006, D2007 and of the latches D2012, D2013 and of the datarams D2018, D2019 may be compared by means of a logic scope, to locate the defective circuit element.

Check whether D2006/7, pins 1-19 are at zero level during the test. If not, use test module 6 to verify.



TEST 5

MA10369

Fig. 4. Flow chart of test 5

2.2.4. Test 6. Signals for data input control. See fig. 5.

With the testmodule 6 a check can be performed on the effect of the commands "HLTDI" and "STRDI". This is done by checking the "WRAM" signal by the program.

The "WRAM" signal is tested after the "HLTDI" command and after the command "STRDI".

The entire program loop is repeated until a failure is produced or "START/STOP" is pressed to request for next testmodule.

When a failure is produced the loop is shortcut to the display function, displaying "TEST 6 FAILS", in order to catch incidentally occurring failures.

Pressing "SELECT" (or "0" for one run) restores the entire loop to enable observing systematic failures by means of suitably probing the hardware circuits around the bistable D2023. (pin 8/13). Or examining the effect of instructions of the module on the circuit by means of a logic scope (see 2.3.3.).

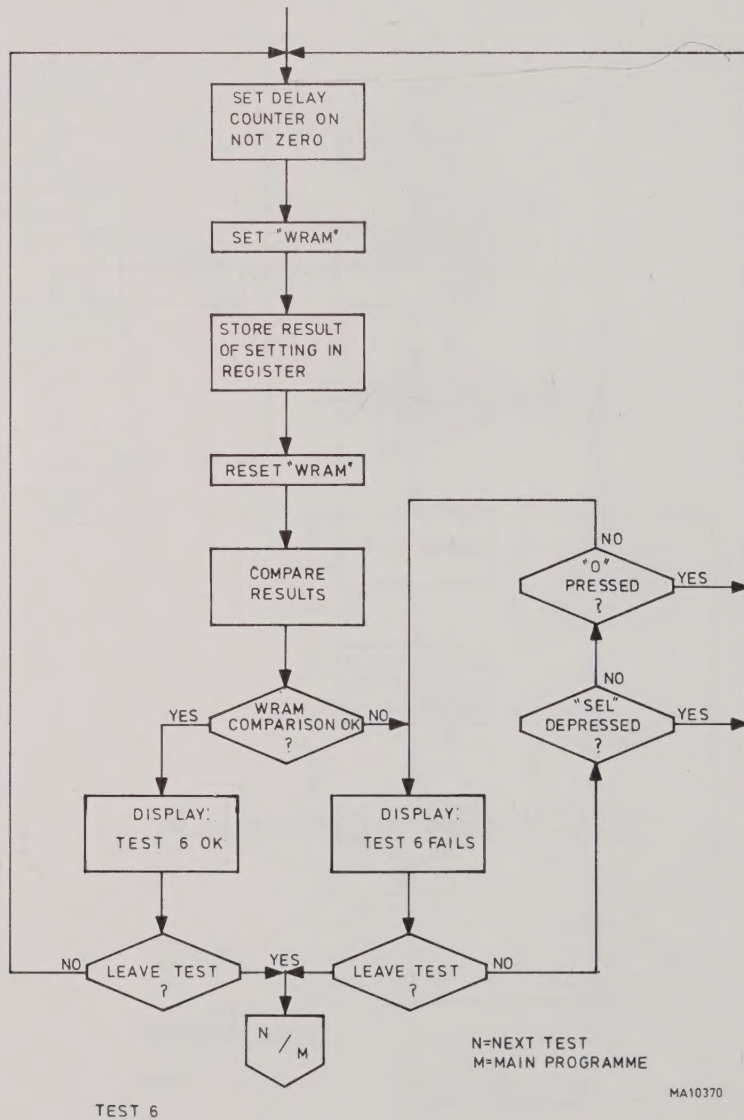


Fig. 5. Flow chart of test 5

2.3. FAILURE TRACING VIA THE SELFTEST

2.3.1. Failing of the display

If the instrument, when switched on, does not show character display in LSA mode, then verify:

- That the cathode-ray tube circuit and the time-base generator are operating correctly.
To check this switch to OSC.-mode and adjust with potmeters FOCUS, INTENS and POSITION for a well-defined display.
If no result is obtained then check the oscilloscope tube-biasing and -functioning procedures as has been described for the oscilloscope (for this, see the manual).
- The functioning of the testprogram.
To check this switch on the testing program by pressing STORE REF and STORE TRIG simultaneously.
Verify whether pulse activities are present with an oscilloscope or analyzer at:
D2008, pins 5 and 6.
D2069, pins 1, 2 and 3.
- The controls signals not to be zero.
Check RDIM and MATRIX (D2063, pins 14, 11).
And the READY signal (D2059, pin 35).
- The micro-processor to function correctly.
This can be tested in free running mode, see chapter 4.

Note: The program may have been interrupted by a trivial interference and hold up in some loop. Therefore try always a second switching on of the instrument.

2.3.2. Failing of functional tests

The following procedure is given as an aid to optimize your diagnosis. A combination of failing tests can give a clearer indication of the faulty circuitry. All functional test modules should be checked before any conclusion is drawn.

- Test 2, 3 OK with CNT = 0000
- Test 5 Failing at all addr.
- Test 6 Failing
- Test 7, 8 Failing at odd resp. at even addr. alternatively.
 Check if "WRAM" is drawn to zero.
 D2022, pin 9.
 Check D2023, pins 8, 9, 10, 13 and so on at test 7, 8.
 Check further Test 6 hardware diagram.

- Test 2, 3 Failing with overflow. CNT = 9986
- Test 6 Failing
- Test 7, 8 Failing at odd/even addr.
 Check if "WRAM" is drawn to high level at test 7, 8:
 D2032, pin 8
 Check further Test 6 hardware diagram.

- Test 2, 3 OK with CNT = 0000
- Test 4 Failing at all addr.
- Test 5 Failing at all addr.
- Test 7, 8 Failing at odd/even addr.
 Check "SYSCL" with an oscilloscope
 D2036, pins 1-6

- Test 2, 3 OK with CNT = 0000
- Test 5 Fails at all addr.
- Test 7, 8 Failing at odd/even addr.
 Check at test 7/8, D2021, pin 3
 D2022, pin 2
 D2029, pin 3
 D2033, pin 8
 Check "SYSCL" with an oscilloscope

- Test 2, 3 Failing with overflow (9986)
- Test 7, 8 Failing at odd/even addr.
 Check at test 7/8
 D2009/D2011, pin 6
 D2008, pin 11
 Check at test 2/3
 D2023 pins 1-6 or
 D2024, pin 12
 D2031, pins 5, 6
 D2032, pins 5, 4
 D2036, pins 8-13.

- Test 4 Failing at all addr.
- Test 5 Failing at all addr.
 Check if "RDIM" (D2014, pin 11, etc.)
 remains high and is not pulsating.

2.4. HINTS FOR DETECTING FAULTS IN CIRCUITRY NOT COVERED BY THE SELFTEST

2.4.1. Failures in the Display circuitry

For tracing failures in the display circuitry no tests provided. These failures can be recognized easy during normal operation and traced by means of signature analysis, oscilloscope or analyzer.

- Line and character position, the horizontal and vertical deflection are controlled by DAC-signals.
The vertical deflection can be checked with an oscilloscope by probing at points R2106/R2104/R2107 and zero-level. Depending on the contents of the screen a staircase pattern is shown with a maximum of 23 steps.
- The horizontal deflection can be checked with an oscilloscope by probing at points X25-6 and X25-4 or/and at R2157/R2156/R2158 and zero-level. The staircase pattern has now a maximum of 32 steps.
- The latch inputs and outputs of latch D2077 can be checked by an oscilloscope.
By means of a logic analyzer the ASCII-codes can be checked.
- Decoder D2077 and character generator D2076 can both be checked by a logic analyzer.
- Z-mod gate D2008.
Check by comparing the signals on pin 5 and pin 6 on different signals.
- The parts of the circuitry not described can be checked, during display operation, by an oscilloscope.
- The SID-pin of the μ P must have zero-level when the LSA mode is selected.

2.4.2. Clockpulse circuit

"SYSCL" pulses are too short to be discerned by S.A. directly.

The presence of them is however indicated by the status of the bistables and thence by the signatures and the flickering of the probe lamp.

To observe "SYSCL" pulses use an oscilloscope on D2036 pin 5 e.g. triggered by the read/write signal leading edge.

"SYSCL" pulses are generated by a "CLDIM" signal during test 4.

If this is failing then test 4 claims a failing test at all addresses of the dataram addresscounter.

For the PM 3540/03 also tests 7 and 8 will in that case display a failure at alternative addresses.

During test 2 and 3, "SYSCL" is generated by latch pulses.

Overflow and failure is displayed when "SYSCL" pulses are missing.

2.4.3. Testing with the logic scope

If a logic scope is available, connect the input terminals to the data and address lines of the 8085 bus system of the tested instrument. Derive a clock pulse from the read and/or write signal of the microprocessor.

Triggering of the logic scope can be adjusted by selecting an appropriate delaytime after determining the triggerword from the program listing.

Any other external oscilloscope can be used if necessary and triggered by deriving a signal from X-18 of the measuring logic scope. In this way the effect of a particular instruction on the circuit can be examined and the circuit tested.

Circuit outputs can be displayed simultaneously if connected to the logic scope input terminals (use one L.S.B.).

3. SIGNATURE ANALYSIS MODE

3.1. GENERAL INFORMATION

Signature Analysis is used in preference in combination with functional testing. A functional test may determine the hardware area that contains the defect or defective component. The number of signatures to be tested can then be reduced considerably. Finding the source of the faulty signatures will however not always lead straight to the defective component. In case more IC's are connected to one wire (WIRE-AND Mode) and/or if one short circuited in- or output caused the damage of another, it will need some closer testing with additional means, e.g. using a logic pulser and a current tracer and/or a sensitive oscilloscope may reveal the direction of (short-circuit) currents or pulse voltage drops. The most difficult defects are caused by IC's that are deteriorating and beginning to produce high voltage drops or high leakage currents and too slow rise and fall times. With the aid of an oscilloscope this type of defects can best be traced.

- Other fault finding aids are:
- Logic probe (S.A. probe) : to detect the presence of pulses and logic levels.
 - Logic clip : to see the functioning of a particular IC on LED display.
 - Logic comparator : to compare any particular IC with an external one getting the same input and power supply.

3.2. SELECTION OF THE S.A. MODE

When all the test modules are observed and conclusions are drawn the failure can be traced by means of signature analysis. In order to generate stable signatures each test module must be set in a loop. This is done by selecting the failing test module and depressing the pushbutton AUTO. Then signatures are generated in the section of the circuitry enclosed by the selected test. Be aware that only in that particular section of the circuitry the signatures can be used for comparison. The functional test program can be re-entered by releasing the AUTO push-button.

3.3. CONNECTIONS AND SETTINGS

In order to get the right signatures the connection of the Signature Analyzer to the Logic Scope should always be the same.

- | | | |
|-------------|---------|---|
| Connections | : START | : D2059 - pin 34, I/O signal from microprocessor |
| | STOP | : D2059 - pin 34, I/O signal from microprocessor |
| | CLOCK | : D2051 - pin 11, Read/Write signal of microprocessor |
| Settings | : START | : negative going edge  |
| | STOP | : positive going edge  |
| | CLOCK | : positive going edge  |

3.4. FAILURE TRACING WITH S.A.

Select the failing test module and depress the pushbutton AUTO. Then signatures are generated in the circuitry enclosed by this test.

The signatures can be traced by using the following hardware diagrams.

The first column indicates the IC numbers dealing with the main stream of data, the second and third column indicate the IC numbers for substreams of data. The procedure is roughly:

Start checking and comparing signatures at the first column downwards and move horizontally to the second column and downwards when failures are no longer observed in the first, etc. Consult the wiring diagram when aberrations in the procedure appear to be necessary.

Note: The display circuitry can be checked with signature analysis in test module 5.

So in that module can not only the signatures of the Data Acquisition Memory, but also the display circuitry be checked.

All pushbuttons must be released except LSA/OSC and AUTO.

D2031, pin 8 drawn to zero or D2033, pin 8 drawn high will not be detected by the functioned tests.

Signatures at these points are changed then.

These errors cause continuous "SYSCL" pulses giving rise to mutilation of data at normal operation.

TEST 2 AND 3

I	II	III
D2023 p8-13		
	D2024	
		D2063 p12, etc.
	D2032 p1,2,3,11,12,13	
		D2039 p1, 2
D2032 p4, 5, 6		
	D2036 p1-5	
D2031 p1-6		
	D2023 p1-6	
D2026		
D2027		
D2028		
	D2024	
	D2008, p8, 9, 10	D2036, p8-13

List of signatures of this test is given in chapter 3.5.

TEST 4

I	II	III
D2014 D2017	D2016 p4, 5, 6 D2036 p1-5 D2063 p1-6, 14	
D2062	D2059 μ P	

List of signatures of these tests is given in chapter 3.5.

TEST 5

I	II	III
	D2053 D2054 p4, 7, 9, 12 D2056 2, 14, 1, 15 D2057	D2051 p4, 5, 6 D2062
D2018 D2019	D2016 p1, 2, 3, 11 12, 13 D2014 D2017	
D2012 D2013	D2036 p1-5	
D2006 D2007	D2023 p8-13	

List of signatures of these tests is given in chapter 3.5.

TEST 6

I	II	III
D2023 p8-13	D2024 (see test 2) pin 12 D2032 p1, 2, 3	D2039 p1,2 D2032 p11, 12, 13
D2022 p8, 9, 11	D2032 p4, 5, 6 D2063 p1-6, 15	D2062

List of signatures of these tests is given in chapter 3.5.

TEST 7 and 8

I	II	III
	<i>check on "SYSCL"</i> D2036 p1-5	
D2009 D2011		D2034 p1, 2, 3, 11 12, 13
	D2008 p1, 2, 3, 11 12, 13	
D2003 D2004		
	D2023 p8-13	

List of signatures of this test is given in chapter 3.5.

3.5. LIST OF SIGNATURES

Signatures test 2 and 3

D2023	1	62A2	D2026	13	9752	D2028	13	A85U	D2036	9	0000
	2	0000		14	2581		14	HU24		10	62A2
	3	0000		15	CAP6		15	CAP6		11	0000
	4	0305		16	62A2		16	62A2		12	62A2
	5	4247	D2027	1	HHC5	D2024	1	HHC5	D2008	13	62A2
	8	U450		2	48UH		2	8HA6		8	O305
	9	96U2		3	2002		3	U9C7		9	O305
	10	62A2		4	0000		4	4247		10	A52A
	11	U709		5	62A2		5	62A2	D2063	12	O305
	12	4723		6	H14U		6	P534		13	P777
	13	O223		7	C983		7	CCIC		14	62A2
D2032	4	U709		8	0000		8	0000		15	A6A0
	5	95AC		9	42U3		9	42U3		16	62A2
	6	0000		10	A2AA		10	A2AA	D2039	1	O223
D2031	1	CPP6		11	0305		11	O305		2	6081
	2	9P70		12	CPP6		12	4723			
	3			13	HU24		13	2581			
	4	8HHA		14	9752		14	0000			
	5	20P5		15	5H41		15	5H41			
	6	95AC		16	62A2		16	62A2			
D2026	1	661A	D2028	1	661A	D2032	1	O223			
	2	6HHC		2	29P2		2	6081			
	3	PP1C		3	0811		3	0000			
	4	0000		4	0000		11	0000			
	5	62A2		5	62A2		12	62A2			
	6	7555		6	6FP8	D2036	13	0000			
	7	4HFC		7	2HU8		1	62A2			
	8	0000		8	0000		2	94H1			
	9	9UA4		9	9UA4		3	215F			
	10	52CA		10	52CA		4	62A2			
	11	0305		11	0305		5	0000			
	12	9P70		12	8HHA		8	62A2			

Signatures test 4

D2014	1	U7HC	D2062	2	38PC	D2063	14	C4U8	D2059	33	F7U4
	2	OU7P		3	32FU					34	0000
	3	3P12		4	P156	D2059	1			35	P7CP
	4	0000		5	H1H4		2			36	P7CP
	5	0000		6	C7P2		3	0000		37	P7CP
	6	3109		7	A9U8		4	0000		38	0000
	7	55H8		8	1F65		5	0000		39	0000
	8	0000		9	U7HC		6	0000		40	P7CP
	9	C7P2		10	0000		7	0000			
	10	P779		11	0000		8	0000			
	11	C4U8		12	U27A		9	P7CP			
	12	7805		13	9985		10	0000			
	13	9UCC		14	94AH		11	P7CP			
	14	8026		15	P779		12	9985			
	15	U27A		16	HA72		13	1F65			
	16	P7CP		17	P145		14	94AH			
D2017	1	H1H4		18	FH8H		15	A9U8			
	2	0000		19	H6A9		16	P145			
	3	C53H		20	P7CP		17	P156			
	4	9UCC	D2016	4	9UCC		18	FH8H			
	5	0000		5	7805		19	32FU			
	6	0000		6	7805		20	0000			
	7	0000	D2036	1	6798		21	U8C8			
	8	0000		2	0000		22	3A3C			
	9	0000		3	6F71		23	7P99			
	10	0000		4	6798		24	76F1			
	11	C4U8		5	8026		25	COOP			
	12	0000	D2063	1	76F1		26	9048			
	13	P7CP		2	COOP		27	0000			
	14	8026		3	9048		28	779H			
	15	HA72		4	0000		29	OC13			
	16	P7CP		5	0000		30	0000			
				6	779H		31	P7CP			
D2062	1	0000					32	P7CP			

Signatures test 5

D2018	1	6F95	D2012	1	0000	D2006	17		D2016	1	0U7C
	2	227H		2	10U9		18	10U9		2	1932
	3	H81U		3	10U9		19	0000		3	COP1
	4	10U9		4	10U9		20	10U9		11	345A
	5	10U9		5	10U9	D2007	1	0000		12	COP1
	6	10U9		6	10U9		2			13	AU63
	7	10U9		7	10U9		3	10U9	D2014	1	99CF
	8	10U9		8	10U9		4			2	H81U
	9	10U9		9	10U9		5	10U9		3	6F41
	10	10U9		10	0000		6			4	0000
	11	10U9		11	0000		7	10U9		5	0000
	12	10U9		12	10U9		8			6	9682
	13	0000		13	10U9		9	10U9		7	227H
	14	0000		14	10U9		10	0000		8	0000
	15	0U7C		15	10U9		11			9	6HHH
	16	0000		16	10U9		12	10U9		10	7124
	17	0000		17	10U9		13			11	COP1
	18	0000		18	10U9		14	10U9		12	UF84
	19	0000		19	10U9		15			13	PF7H
	20	0000		20	10U9		16	10U9		14	0000
	21	0000	D2013	1	0000		17			15	345P
	22	0000		2	10U9		18	10U9		16	10U9
	23	0000		3	10U9		19	0000	D2017	1	300A
	24	0000		4	10U9		20	10U9		2	6F95
	25	6F41		5	10U9	D2053	1	P354		3	U535
	26	9682		6	10U9		2	70HH		4	PF7H
	27	U535		7	10U9		4	0000		5	0000
	28	10U9		8	10U9		7	553A		6	5F5A
D2019	1	6F95		9	10U9		9	60H3		7	0000
	2	227H		10	0000		12	0000		8	0000
	3	H81U		11	0000		14	24FA		9	0000
	4	10U9		12	10U9		15	P354		10	0000
	5	10U9		13	10U9	D2054	1	P354		11	COP1
	6	10U9		14	10U9		2	70HH		12	0000
	7	10U9		15	10U9		4	0000		13	10U9
	8	10U9		16	10U9		7	PCH8		14	0000
	9	10U9		17	10U9		9	3APU		15	6966
	10	10U9		18	10U9		12	0000		16	10U9
	11	10U9		19	10U9		14	24FA	D2036	1	10U9
	12	10U9		20	10U9		15	P354		2	7C5F
	13	0000	D2006	1	0000	D2056	1	P354		3	9HP6
	14	0000		2			2	70HH		4	10U9
	15	AU63		3	10U9		4	0000		5	0000
	16	AU63		4			7	51FP	D2023	8	10U9
	17	0000		5	10U9		9	C2P8		9	0000
	18	0000		6			12	0000		10	10U9
	19	0000		7	10U9		14	24FA		11	0000
	20	0000		8			15	P354		13	7C5F
	21	0000		9	10U9	D2057	1	P354	D2051	4	COP1
	22	0000		10	0000		2	70HH		5	434F
	23	0000		11			4	0000		6	P354
	24	0000		12	10U9		7	P7F9	D2062	1	0000
	25	6F41		13			9	2H90		2	70HH
	26	9682		14	10U9		12	0000		3	2H90
	27	U535		15			14	24FA		4	P7F9
	28	10U9		16	10U9		15	P354		5	300A

Signatures test 5 cont.

D2062	6	6HHH	5	C9HA	D2079	1	10U9
	7	C2P8	6	60H3		2	F58P
	8	3APU	7	8742		3	PCH8
	9	99CF	8	0000		4	553A
	10	0000	9	CF1U		5	3P71
	11	0000	10	6U5H		6	60H3
	12	345P	11	3APU		7	P4H4
	13	60H3	12	0000		8	0Q00
	14	553A	13	C2P8		9	844F
	15	7124	14	PCH8		10	0000
	16	6966	15	H4C8		11	2H90
	17	PCH8	16	10U9		12	UF6H
	18	51FP	D2071	1		13	3APU
	19	24FA		2		14	C2P8
	20	10U9		3		14	H730
				4		16	10U9
D2077	5	60C7	5	5850	D2058	1	10U9
	6	704P	6	48A9		2	10U9
	7	0000	7	0000		3	10U9
	8	0000	8	A9U8		4	10U9
	10	AF7C	9	C901		5	10U9
	11	71F8	10	10U9		6	10U9
	12	0000	11	10U9		7	0000
	16	10U9	12	A9U8		8	10U9
D2072	1	5850	13	10U9		9	10U9
	2	F3F0	14	10U9		10	10U9
	3	10U9	D2069	1		11	10U9
	4	10U9		2		12	10U9
	5	0000		3		13	10U9
	6	71F8		4		14	10U9
	7	3671		5			
	8	0000		6			
	9	10U9		7			
	10	0000		8			
	11	AF7C		9			
	12	10U9		10			
	13	10U9		11			
	14	4762		12			
	15	C901		13			
	16	10U9		14			
D2073	1	5850	D2008	4	0000		
	2	0000		5	60C7		
	3	0000		6	60C7		
	4	0000	D2078	1	10U9		
	5	3671		2	7AF3		
	6	H326		3	PCH8		
	7	P799		4	553A		
	8	0000		5	HP9U		
	9	10U9		6	60H3		
	10	0000		7	7CC1		
	11	HHA0		8	0000		
	12	10U9		9	COUH		
	13	0000		10			
	14	0000		11			
	15	C901		12	HF0A		
	16	10U9		13	3APU		
D2074	1	10U9	14	C2P8			
	2	2F5P	15	431C			
	3	P7F9	16	10U9			
	4	553A					

Signatures test 6

D2023	8	805F
	9	P6FP
	10	A9UF
	11	0000
	12	0000
	13	4F05
D2022	8	7AH7
	9	A9U7
	11	3720
D2024	12	0000
D2032	4	0000
	5	6692
	6	FU6P
	11	0000
	12	6692
	13	0000
D2063	1	OC17
	2	9888
	3	3CP8
	4	0000
	5	0000
	6	HU9A
	15	3720
D2039	1	4F05
	2	2A97

D2062	1	0000
	2	939U
	3	F1UU
	4	PF71
	5	29C6
	6	CFP1
	7	APH3
	8	7AH7
	9	6756
	10	0000
	11	0000
	12	U86H
	13	889F
	14	H5A2
	15	6088
	16	U053
	17	706P
	18	9UU8
	19	939U
	20	6692

Signatures test 7, 8

D2009	1	0H29	D2003	2	1729	D2004	15	5P96
	2	69CC		3	0H29		16	69CC
	3	0000		4	69CC		17	0H29
	4	0000		5	5P96		18	1729
	5	0000		6	P4HP		19	0000
	6	40AA/8U83		7	C7U4		20	0F4U
	7	4F00		8	P40F	D2036	1	1ACU
	8	0000		9	4F00		2	0000
	9	P40F		10	0000		3	0000
	10	P4HP		11	4F00		4	1ACU
	11	C7U4		12	P40F		5	16U0
	12	FH91		13	C7U4	D2008	1	AH15
	13	6H5C/C895		14	P4HP		2	FH91
	14	5P96		15	5P96		3	FH91
	15	1729		16	69CC		11	FH91
	16	0F4U		17	0H29		12	839P
D2011	1	0H29	D2004	18	1729		13	FH91
	2	69CC		19	0000	D2023	8	0000
	3	0000		20	0F4U		9	0F4U
	4	0000		1	0000		10	0000
	5	0000		2	1729		11	0000
	6	4 0AA/8U83		3	0H29		12	H9HC
	7	4F00		4	69CC		13	0F4U
	8	0000		5	5P96	D2034	1	0F4U
	9	P40F		6	P4HP		2	0000
	10	P4HP		7	C7U4		3	0F4U
	11	C7U4		8	P40F		11	1ACU
	12	FH91		9	4F00		12	0F4U
	13	6H5C/C895		10	0000		13	16U0
	14	5P96		11	4F00			
	15	1729		12	P40F			
	16	0F4U		13	C7U4			
D2003	1	0000		14	P4HP			

4. TESTING THE MICROPROCESSOR AND ADDRESS BUS

The selftest programs can only be used if the microprocessor μP , the EPROMS address- and data bus are functioning well.

If there is any doubt the μP can be replaced or tested externally in free-running mode.

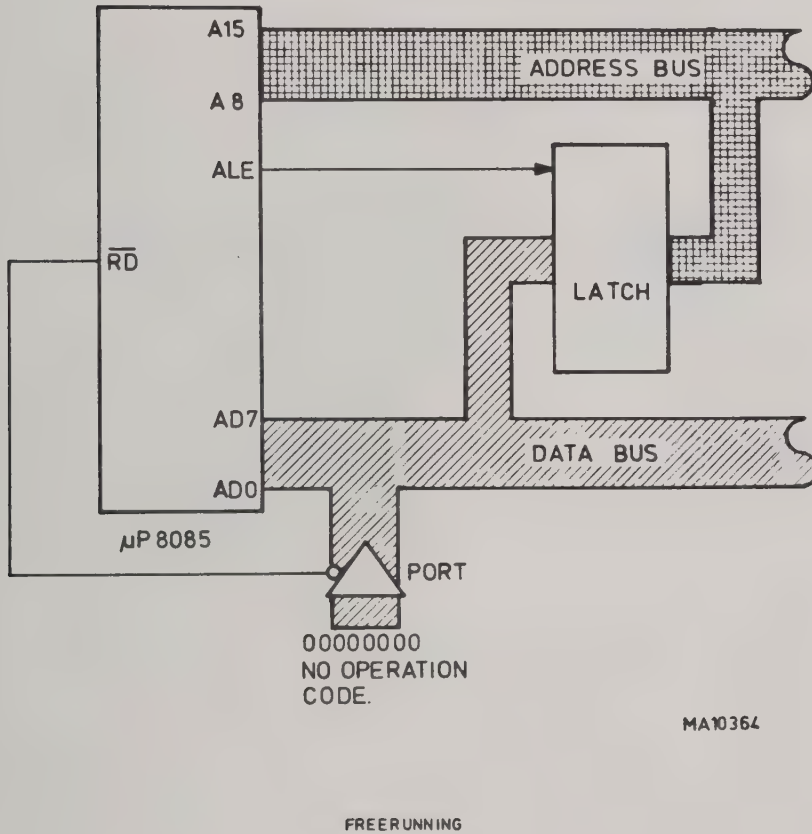


Fig. 7. Free-running

4.1. FREE-RUNNING

The μ P can be tested free-running by connecting the multiplexed address-data bus to ground during the read-cycle. That means that instruction NOP (No Operation) is fed to the μ P. After a reset the μ P starts at address 0000 (Hex) NOP-instruction is read and fed to the μ P. The μ P increments the Program Counter and reads again the same NOP-instruction.

In this mode the Program Counter counts from 0000 to FFFF which can be checked on the address bus by means of a logic analyzer, an oscilloscope or a signature analyzer.

The Logic-Scope PM 3540 is not provided with the facility of disconnecting the address-data bus so that the μ P can only be tested free-running by using an external device.

This facility can be created on an external board using the concept shown mechanically and electronically in figures 8 and 9.

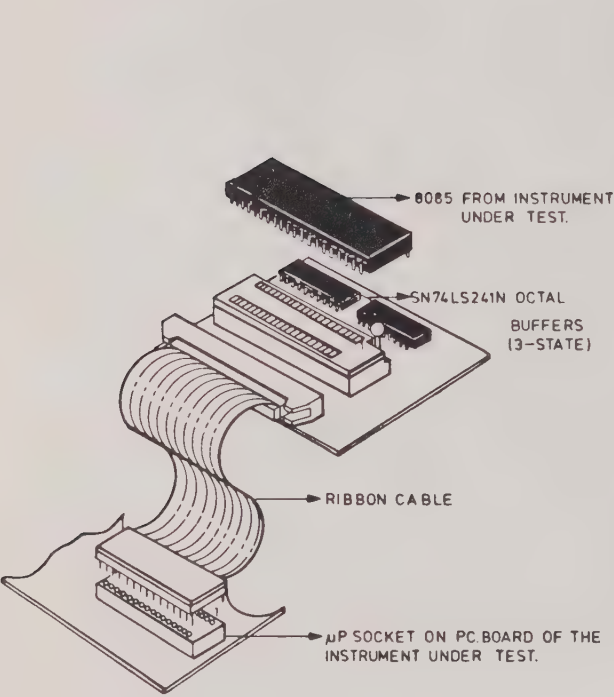


Fig. 8. Free-running test set-up (Mechanical)

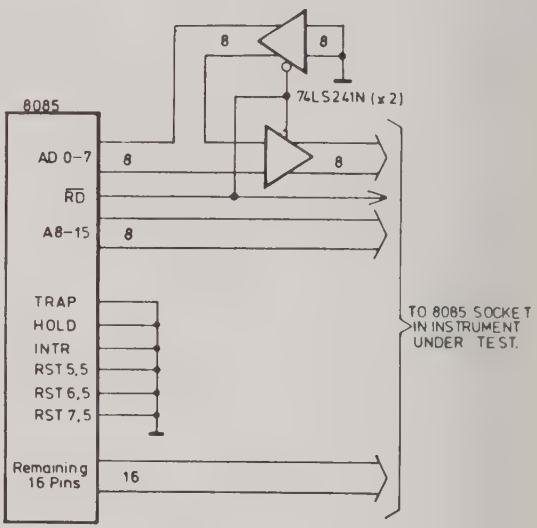


Fig. 9. Free-running test set-up (Electrical)

MA10365

4.2. FREE-RUNNING TEST SET-UP

A plug-in device in accordance to above mentioned concept is currently being developed. For more information concerning this suitable device (which can be used for testing all 8085 μ P-systems) contact N.V. Philips' Gloeilampenfabrieken, Eindhoven, S & I-Service - T & M the group Data Test Equipment.

5. MANUAL CONSEQUENCES DUE TO MODIFICATIONS

The following text refers directly to the appropriate sections in the manual. (no. 9499 503 00402).

1.2.2.2. Vertical amplifier

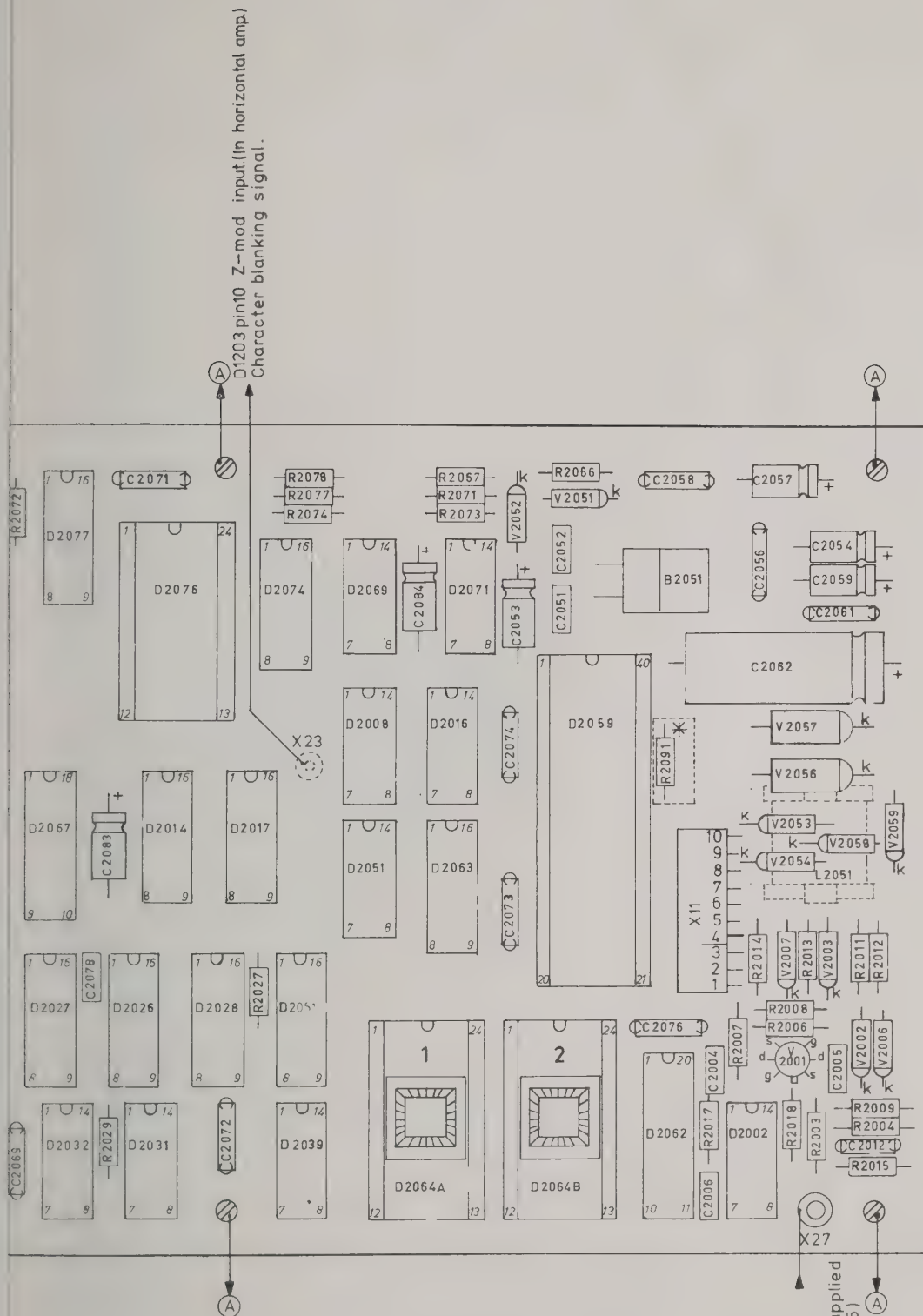
Frequency range	DC : 0 ... 35 MHz (−3 dB) AC : 2 Hz ... 35 MHz (−3 dB)	
Rise Time	≤ 10 ns	
Pulse aberrations	≤ ± 3 % (≤ 4 % pp)	Measured at 6 div. amplitude and applied rise time of ≥ 1 ns

1.2.2.4. Triggering

Trigger sensitivity	Internal : 1.0 DIV. at 35 MHz External: 0.2 Vpp at 35 MHz TV int. : 0.7 DIV TV ext.: 0.15 Vpp	Sync pulse amplitude Sync pulse amplitude
Triggering frequency range	AUTO : 20 Hz ... ≥ 35 MHz AC : 5 Hz ... ≥ 35 MHz DC : 0 Hz ... ≥ 35 MHz	Typically, stable triggering can stil be obtained at 50 MHz and 2 div. or 1 Vpp amplitude.

3.8. INTEGRATED CIRCUITS

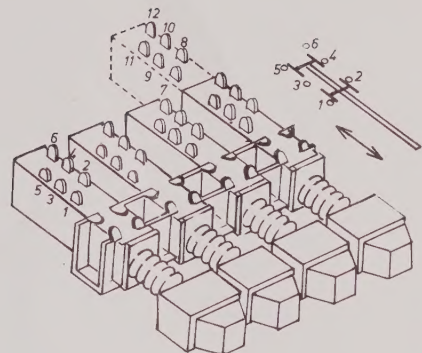
D2064 (A & B)	PROMset programmed	5322 209 14774	versions /01 and /02
D2064 (A & B)	PROMset programmed	5322 209 14782	versions /03 and onwards



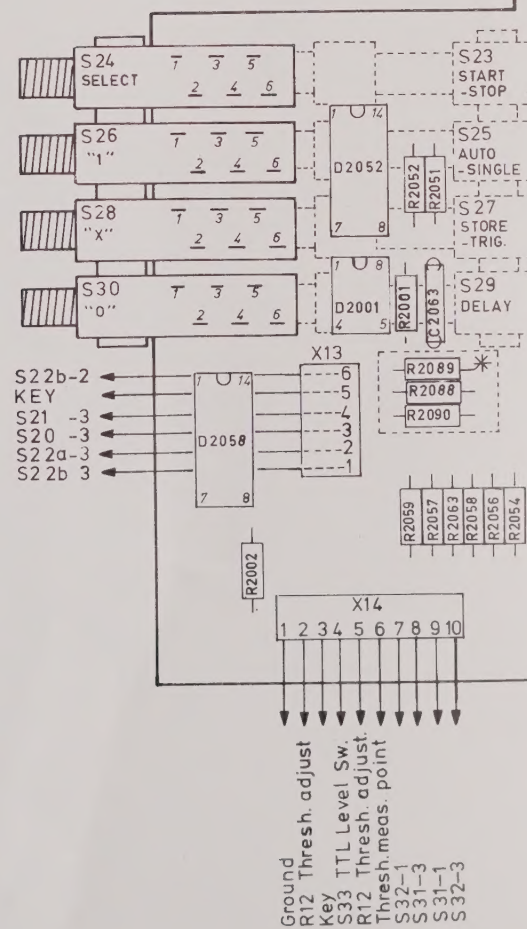
To Switch DATA
S16 contact 11
(EXT. TRIG. signal applied
to front socket X5)

* These components model 03 onwards.

Fig. 10. Micro-processor p.c. board



Typical switch arrangement



- Ground
- R12 Thresh. adjust
- Key
- TTL Level Sw.
- S33 Thresh. adjust
- R12 Thresh. adjust
- Thresh. meas. point
- S32-1
- S31-3
- S31-1
- S32-3

www.manualsplus.com



1011014